## AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Previously Presented) An integrated circuit structure, comprising:

a capacitive electrode proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is placed on the sensing surface;

a dielectric underlying the capacitive electrode; and

an active region underlying the dielectric,

wherein the capacitive electrode and all conductive regions between the capacitive electrode and the active region are formed of a conductive material having a hardness greater than a hardness of aluminum.

2. (Original) The integrated circuit structure of claim 1, wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness at least as great as a hardness of the dielectric.

3. (Previously Presented) The integrated circuit structure of claim 1, further comprising:

a passivation layer over the capacitive electrode, the passivation layer forming the sensing surface,

wherein the capacitive electrode and all conductive regions between the capacitive electrode and the active region are formed of a conductive material having a hardness at least as great as a hardness of the passivation layer.

4. (Previously Presented) The integrated circuit structure of claim 1, wherein the capacitive electrode and all conductive regions between the capacitive electrode and the active region are formed of tungsten.

5. (Original) The integrated circuit structure of claim 4, further comprising:

a tungsten via beneath the capacitive electrode.

6. (Original) The integrated circuit structure of claim 5, further comprising:

a tungsten interconnect beneath the via.

7. (Original) The integrated circuit structure of claim 6, further comprising:

a tungsten contact between the interconnect and the active region.

8. (Original) The integrated circuit structure of claim 7, wherein the active region is a gate electrode.

9. (Previously Presented/Withdrawn) An integrated circuit structure, comprising:

an active region;

a dielectric overlying the active region and having a contact opening therethrough;

a tungsten contact within the contact opening;

a tungsten metal region overlying the contact and a portion of the dielectric;

an interlevel dielectric overlying the tungsten metal region and the dielectric and having an opening therethrough;

a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel dielectric, wherein the capacitive electrode is proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is place on the sensing surface and is electrically connected to the active region by the contact, the metal region, and the via.

Claims 10-13 (Canceled)

14. (Previously Presented) A method of forming a scratch resistant integrated circuit structure, comprising:

forming an active region;

forming a dielectric overlying the active region; and

forming a capacitive electrode overlying the dielectric proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is placed on the sensing surface, wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness greater than a hardness of aluminum.

15. (Original) The method of claim 14, wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness at least as great as a hardness of the dielectric.

16. (Previously Presented) The method of claim 14, further comprising:

forming a passivation layer over the capacitive electrode, the passivation layer forming the sensing surface,

wherein the capacitive electrode and all conductive regions between the capacitive electrode and the active region are formed of a conductive material having a hardness at least as great as a hardness of the passivation layer.

17. (Previously Presented) The method of claim 14, wherein the capacitive electrode and all conductive regions between the capacitive electrode and the active region are formed of tungsten.

18. (Original) The method of claim 17, further comprising:

forming a tungsten via beneath the capacitive electrode.

19. (Original) The method of claim 18, further comprising:

forming a tungsten interconnect beneath the via.

20. (Original) The method of claim 19, further comprising:

forming a tungsten contact between the interconnect and the active region.

21. (Original) The method of claim 20, wherein the active region is a gate electrode.

22. (Previously Presented/Withdrawn) A method of forming an integrated circuit structure, comprising:

forming an active region;

forming a dielectric overlying the active region and having a contact opening therethrough;

forming a tungsten contact within the contact opening;

forming a tungsten metal region overlying the contact and a portion of the dielectric;

forming an interlevel dielectric overlying the tungsten metal region and the dielectric and having an opening therethrough;

forming a tungsten via within the opening through the interlevel dielectric; and

forming a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel dielectric, wherein the capacitive electrode is proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is placed on the sensing surface and is electrically connected to the active region by the contact, the metal region, and the via.

23. (Original/Withdrawn) The method of claim 22, further comprising:

forming an oxide over the capacitive electrode and the interlevel dielectric adjacent the capacitive electrode;

forming a passivation layer including a silicon nitride layer and a silicon carbide layer over the oxide; and

forming tungsten ESD protection within the passivation layer.

24. (Previously Presented) A method of forming a scratch resistant integrated circuit structure, comprising:

forming a plurality of active regions;

forming a dielectric over the plurality active regions; and

forming an array of capacitive electrodes overlying the dielectric proximate to a sensing surface on which an object is selectively placed, the capacitive electrodes each forming a capacitor with the object when the object is placed on the sensing surface and wherein the capacitive electrodes are each formed of a conductive material having a hardness at least as great as a hardness of the dielectric.

25. (Previously Presented) The method of claim 24, wherein the step of forming an array of capacitive electrodes overlying the dielectric of a conductive material having a hardness at least as great as a hardness of the dielectric further comprises:

forming the array of capacitive electrodes of a conductive material having a hardness at least as great as a hardness of a passivation layer overlying the array of conductive electrodes and forming the sensing surface.

26. (Original) The method of claim 24, wherein the step of forming an array of capacitive electrodes overlying the dielectric of a conductive material having a hardness at least as great as a hardness of the dielectric further comprises:

forming the array of capacitive electrodes of tungsten.

27. (Original) The method of claim 24, further comprising:

forming each metallization region between the array of capacitive electrodes and the plurality of active regions of a conductive material having a hardness at least as great as the hardness of the dielectric.